hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

Date: January 8, 2004

ATES PATENT AND TRADEMARK OFFICE

Applic. No.

10/723,907

Applicant

Marie Denison

Filed

November 26, 2003

Art Unit

to be assigned

Examiner

to be assigned

Docket No.

MUH-12869

Customer No.:

24131

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner for Patents

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

B. Jayant Baliga: "Modern Power Devices", Krieger Publishing Company, Malabar, Florida, 1987, pp. 81, 83 and 88;

Taylor Efland: "Lateral DMOS Structure Development for Advanced Power Technologies", TI Technical Journal, March/April 1994, pp. 10-24;

S. Merchant et al.: "High-Performance 13-65 V Rated LDMOS Transistors in an Advanced Smart Power Technology", IEEE, 1999, pp. 225-227.

Respectfully submitted,

bligant

January 8, 2004

rner And Greenberg, P.A.

Post Office Box 2480

Hollywood, FL 33022-2480

Tel: (954) 925-1100 Fax: (954) 925-1101

/bmb

Gregory L. Mayback Reg. No. 40,719

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U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))

Attorney Docket N	10
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Applicant

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November 26, 2003

U.S. PATENT DOCUMENTS

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

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Р	Taylor Efland: "Lateral DMOS Structure Development for Advanced Power Technologies", TI Technical Journal, March/April 1994, pp. 10-24

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